Elec/Comp 526
Spring 2014
High Performance Computer Architecture

- Instructor

  Peter Varman

  DH 2022 (Duncan Hall)

  pjv @ rice.edu x3990

- Office Hours

  Tue/Thu 1- 3 pm or

  By Appointment

- Web Page

  OWLSPACE: Elec/Comp 526 Spring 2014

Elec/Comp 526

Goal

Develop an advanced understanding of modern high-performance computer architectures with an emphasis on parallel systems

Course Material

- Computer Architecture: A Quantitative Approach, (4th edition), J. Hennessy and D. Patterson
- Parallel Computer Organiztion and Design, M. Dubois, M. Annavaram, P. Stenström
- Parallel Computer Architecture: A Software/Hardware Approach, D. Culler and J. P. Singh
- Survey and Research Papers (Will be posted as needed)

Grading

4 Projects (Architecture Simulation) 80% + 1 Exam 20%

Processors

- Instruction Level Parallelism:
  - Review of Simple pipelined processors
  - Register Renaming
  - Memory Disambiguation
  - Dynamically Scheduled OOO processors
  - Tomasulo's Algorithm
  - Superscalar and VLIW processors
  - Branch Prediction
  - Speculative Processing

- Data Parallelism
  - Identical operations on elements of large arrays (vectors)
    - Vector and Stream Processors, GGPUs

- Thread Level (Process Level) Parallelism
  - Application must be written as multiple cooperating threads
    - Multithreaded Processors
    - Shared Memory Multiprocessors: CMP, SMP, NUMA
    - Cluster Computing: Commodity and Custom clusters

Memory Systems

High-Performance Single CPU Memory

- Review of uniprocessor cache organizations
  - Cache optimizations
  - Lockup-free caches

- Multiprocessor Caches
  - Cache Coherence
    - Snooping Protocols
      - MSI cache coherence protocol
      - MESI and MOESI protocols
    - Scalable Cache Coherence
      - Distributed Cache Coherent NUMA systems

- Memory Orderings and Consistency

- Virtual Memory
  - TLB and Page Table Organizations
  - Interaction of Virtual Memory and Caches
    - Physical and Virtual Caches
    - Aliasing

Synchronization

Concurrency Control

- Critical Section Problem
- Point-to-point synchronization
- Barrier Synchronization

- Locks
  - Spin Locks
    - Load and Store based locks
    - TAS and Test-and-TAS
    - LL and SC
    - Hardware Transactional Memory

- Barriers
  - Implementation

- Synchronization and Memory Consistency